Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-17 are pending in the application, with claims 1, 4, 8, 11, 15, and 17 being the independent claims. Claims 4, 11, 15, and 17 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Objections to the Claims

At page 2 of the Office Action, claims 15 and 17 were "objected to because of the following informalities: Replace 'though' with 'through' as it appears throughout the subject claims. Appropriate correction is required." Accordingly, Applicants have amended each of claims 15 and 17 to replace each instance of the word "though" with the word "through". Therefore, Applicants respectfully request that the Examiner reconsider and remove his objections to claims 15 and 17.

Rejections Under 35 U.S.C. § 103

At page 2 of the Office Action, claims 1-3, 8-10, and 15-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,793,990 to Jirgal *et al.* (hereinafter "Jirgal") in view of U.S. Patent No. 5,933,021 to Mohd (hereinafter "Mohd"). Applicants respectfully traverse these rejections.

Regarding claims 1-3 and 8-10, independent claim 1 recites (emphasis added):

> A cross link multiplexer bus, comprising:
> a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin port configured to produce said signal; and
> a plurality of interconnects, wherein ***a set of interconnects*** of said plurality of interconnects ***is coupled between a pair of adjacent cross link multiplexers*** of said plurality of cross link multiplexers;
> wherein:
> said signal is configured to be represented as a series of characters, and a character of said series of characters is configured to be represented as a first data bit, a second data bit, and a first control bit;
> ***a first interconnect of said set of interconnects*** is configured to convey said first data bit, ***a second interconnect of said set of interconnects*** is configured to convey said second data bit, and ***a third interconnect of said set of interconnects*** is configured to convey said first control bit; and
> said first interconnect, said second interconnect, and said third interconnect are configured in a manner to reduce cross-talk.

Independent claim 8 recites similar features.

The Office Action at pages two and three contends that:

> Jirgal discloses a cross link multiplexer bus (Fig. 1, a Mux bus architecture), comprising:
> a plurality of cross link multiplexers (Fig. 14, plurality of Mux's 36, 38, 40), said plurality of cross link multiplexers having a destination port configured to receive a signal (input ports for each Mux 36, 38, 40 is the destination port) and an origin port configured to produce said signal (outgoing ports represent origin ports); and
> a plurality of interconnects (Fig. 14, Mux's interconnected via buses and other links as needed between various ports) wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers

> (output of 32 provides input to 36, 38 and 40 via interconnect line as shown in Fig. 14, thus coupling adjacent Mux's);
>
> said signal is capable of being represented as a series of characters (Fig. 4 where signal A is represented as series of characters, col 6 lines 60-67), and a character of said series of characters is configured to be represented as a first data bit, a second data bit, and a first control bit (col 2 lines 15-35); a first interconnect of said set of interconnects is configured to convey said first data bit (Fig. 1, ref. 18, first interconnect A[25:18] conveys first data bit), a second interconnect of said set of interconnects is configured to convey said second data bit (second interconnect a[17:10] conveys second data bit), and a third interconnect of said set of interconnects is configured to convey said first control bit (CPU control line provides the third interconnect that conveys the control bit).

Even if, for sake of argument, first interconnect A[25:18] of figure 1 of Jirgal can be considered to be configured to convey a first data bit, second interconnect A[17:10} of figure 1 of Jirgal can be considered to be configured to convey a second data bit, and the CPU Control line of figure 1 of Jirgal can be considered to convey a control bit, the set of these three interconnects is not coupled between a pair of adjacent cross link multiplexers.

Figure 1 of Jirgal is "a simplified block diagram of a local bus architecture embodiment of the computer system" disclosed by Jirgal. (Jirgal at c. 4, ll. 24 and 25.) Computer system 10 of figure 1 of Jirgal includes ML System Controller 18. Figure 14 of Jirgal is "a simplified block diagram of the multiplex system controller [ML System Controller 18] of FIGS. **1** and **2**." (Jirgal at c. 4, ll. 61 and 62.) In figure 14 of Jirgal, at least CPU CTRL BUS is not coupled between a pair of adjacent cross link multiplexers.

Therefore, Jirgal does not disclose, teach, or suggest a set of interconnects coupled between a pair of adjacent cross link multiplexers and having a first interconnect configured to convey a first data bit, a second interconnect configured to convey a second data bit, and a third interconnect configured to convey a first control bit. Mohd does not overcome this deficiency.

For at least these reasons, each of independent claims 1 and 8 is patentable over Jirgal in view of Mohd. Because each of claims 2, 3, 9, and 10 depends upon independent claims 1 or 8 and because of the additional distinctive features of each of claims 2, 3, 9, and 10, each of these claims is also patentable over Jirgal in view of Mohd.

Regarding claims 15-17, amended independent claim 15 recites (emphasis added):

> In a cross link multiplexer bus, a method for reducing cross-talk, comprising the steps of:
>
> (1) conveying a first bit of a character of a signal through ***a first interconnect of a plurality of substantially parallel interconnects***;
>
> (2) conveying a second bit of the character of the signal through ***a second interconnect of the plurality of substantially parallel interconnects***; and
>
> (3) conveying a power supply voltage through ***a third interconnect of the plurality of substantially parallel interconnects***;
>
> ***wherein the plurality of substantially parallel interconnects are coupled between a pair of adjacent cross link multiplexers*** and said third interconnect is positioned substantially between said first interconnect and said second interconnect in a manner to reduce cross-talk.

Independent claim 17 has been amended in a similar manner.

As stated above, Jirgal does not disclose, teach, or suggest a set of interconnects coupled between a pair of adjacent cross link multiplexers and having a first interconnect configured to convey a first data bit, a second interconnect configured to convey a second data bit, and a third interconnect configured to convey a first control bit. Mohd does not overcome this deficiency.

Therefore, each of independent claims 15 and 17 is patentable over Jirgal in view of Mohd. Because claim 16 depends upon independent claim 15 and because of the additional distinctive features of claim 16, claim 16 is also patentable over Jirgal in view of Mohd.

Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejections of 1-3, 8-10, and 15-17 under 35 U.S.C. § 103(a) and pass these claims to allowance.

Allowable Subject Matter

At page 4 of the Office Action, claims 4-7 and 11-14 "are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims."

Accordingly, Applicants have amended claim 4 to incorporate the features of independent claim 1 and intervening claim 2. Each of claims 5 and 6 remains dependent upon claim 4 and claim 7 remains dependent upon claim 6. Applicants have also amended claim 11 to incorporate the features of independent claim 8 and intervening claim 9. Each of claims 12 and 13 remains dependent upon claim 11 and claim 14 remains dependent upon claim 13.

Therefore, Applicants respectfully request that the Examiner reconsider and remove his objections to claims 4-7 and 11-14 and pass these claims to allowance.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed or accommodated. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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